

1. A processing core comprising:
2. R-number processing pipelines each comprising N-number of processing
3. paths, wherein each of said R-number of processing pipelines are synchronized to operate as a single very long instruction word (VLIW) processing core, said VLIW processing core being configured to process $R \times N$ -number of VLIW sub-instructions in parallel.
4. The processing core as recited in claim 1 wherein said R-number of processing pipelines can be configured to operate independently as separately operating
5. number of processing pipelines comprises S-number of register files, such that said
6. processing core comprises Q-number of M-bit wide registers, and wherein said Q-number of registers
7. within each of said register files are either private or global registers, and wherein a value is written to one of said Q-number of said registers which is a global register within one
8. of said register files, said value is propagated to a corresponding global register in the other
9. register files, and wherein when a value is written to one of said Q-number of said
10. register files, said value is propagated to a private register within one of said register files, said value is not propagated to a corresponding private register in the other register files.
11. 5. The processing core as recited in claim 3 wherein each of said register
12. files comprises Q-number of M-bit wide registers, and wherein said Q-number of registers
13. within each of said register files are either private or global registers, and wherein a value is written to one of said Q-number of said registers which is a global register within one
14. of said register files, said value is propagated to a corresponding global register in the other
15. register files, and wherein when a value is written to one of said Q-number of said
16. register files, said value is not propagated to a corresponding private register in the other register files.
17. 4. The processing core as recited in claim 3 wherein each of said R-
18. number of processing pipelines comprises one register file for every two of said N-number of
19. processing paths, such that $S = N/2$.
20. 3. The processing core as recited in claim 1 wherein each of said R-
21. number of processing pipelines comprises S-number of register files, such that said
22. processing core comprises R \times S-number of register files.
23. 4. The processing core as recited in claim 3 wherein each of said R-
24. number of processing pipelines comprises one register file for every two of said N-number of
25. processing paths, such that $S = N/2$.
26. 5. The processing core as recited in claim 3 wherein each of said register
27. files comprises Q-number of M-bit wide registers, and wherein said Q-number of registers
28. within each of said register files are either private or global registers, and wherein a value is written to one of said Q-number of said registers which is a global register within one
29. of said register files, said value is propagated to a corresponding global register in the other
30. register files, and wherein when a value is written to one of said Q-number of said
31. register files, said value is not propagated to a corresponding private register in the other register files.
32. 6. The processing core as recited in claim 1, wherein a single VLIW
33. processing instruction comprises $R \times N$ -number of P-bit sub-instructions appended together.
34. 7. The processor chip as recited in claim 6, wherein $M=64$, $Q=64$, and
35. $P=32$.
36. 8. The processing core as recited in claim 3 wherein said each of said R-
37. number of processing pipelines comprises an execute stage which includes an execute unit for

3. each of said N-number processing paths, each of said execute units comprising an integer combining unit, a load/store processing unit, a floating point processing unit, or any combination of one or more of said integer processing units, said load/store processing units, and said floating point processing units.
4. processor comprising an integer processing unit, a floating point processing unit, or any combination of one or more of said integer processing units, said load/store processing units, and said floating point processing units.
5. The processing core as recited in claim 4 wherein Q=64, and a 64-bit special register stores bits indicating whether registers in the register files are private registers or global registers, each bit in the 64-bit special register corresponding to one of the registers or register files connected to a bus, and a value written to a global register in one of said register files is propagated to a corresponding global register in the other register files connected to the bus, and a value written to a global register in one of said register files connected to the bus across said bus.
6. The processing core as recited in claim 5 wherein a plurality of said register files are connected together in serial, and a value written to a first global register in a register file is propagated to a second global register in a plurality of said register files connected to the bus.
7. The processing core as recited in claim 6 wherein each register file is connected to a single very long instruction word (VLIW) processing core, said VLIW processing core being configured to process R x N-number of processing pipelines comprising N-number of processor chips or with I/O devices;
8. a single very long instruction word (VLIW) processing core, said VLIW processing core being configured to process R x N-number of processing pipelines comprising N-number of processor chips or with I/O devices;
9. The processing core as recited in claim 8 wherein each of said processing paths, wherein each of said R-number of processing pipelines are synchronized to operate as paths, wherein each of said R-number of processing pipelines each comprising N-number of processor chips, each comprising:
10. an I/O link configured to communicate with other of said one or more processor cores and said I/O links;
11. a communication controller in electrical communication with said processing core and said I/O links;
12. core and said I/O links;

- 13 said communication controller for controlling the exchange of data between a
 14 first one of said one or more processor chips and said other of said one or more processor
 15 chips;
 16 wherein said computer processing architecture can be scaled larger by
 17 connecting together two or more of said processor chips in parallel via said I/O links of said
 18 processor chips, so as to create multiple processing core pipelines which share data
 19 therebetween.
 14. The computer system as recited in claim 13 wherein said R-number of
 15 processing pipelines can be configured to operate independently as separately operating
 16 pipelines.
 17. The computer system as recited in claim 13 wherein each of said R-
 18 number of processing pipelines comprises S-number of register files, such that said
 19 processing core comprises R x S-number of register files.
 16. The computer system as recited in claim 15 wherein each of said R-
 17 number of processing pipelines comprises one register file for every two of said N-number of
 18 processing paths, such that $S = N/2$.
 19. The computer system as recited in claim 15 wherein each of said
 1. register files comprises Q-number of M-bit wide registers, and wherein said Q-number of
 2. registers within each of said register files are either private or global registers, and wherein
 3. registers within each of said register files are either private or global registers, and wherein
 4. when a value is written to one of said Q-number of said registers which is a global register
 5. within one of said register files, said value is propagated to a corresponding global register in
 6. the other of said register files, and wherein when a value is written to one of said Q-number
 7. of said registers which is a private register within one of said register files, said value is not
 8. propagated to a corresponding register in the other of said register files.
 1. 17. The computer system as recited in claim 15 wherein each of said
 2. register files comprises R x N-number of P-bit sub-instructions appended together.
 3. 18. The computer system as recited in claim 13 wherein a single VLIW
 4. processing instruction comprises R x N-number of P-bit sub-instructions appended together.
 5. 19. The computer system as recited in claim 18 wherein M=64, Q=64, and P=32.
 6. 2. P=32, wherein M=64, Q=64, and P=32.

1. The computer system as recited in claim 15 wherein said each of said R-number of processing pipelines comprises an execute stage which includes an execute unit for each of said N-number processing paths, each of said execute units comprising an integer combination of one or more of said integer processing units, said load/store processing unit, a floating point processing unit, a floating point processing unit, a load/store processing unit, a floating point processing unit, said floating point processing unit and said floating point processing unit.
2. The computer system as recited in claim 20 wherein an integer processing unit and a floating point processing unit share one of said register files.
3. The computer system as recited in claim 21 wherein an integer processing unit and a floating point processing unit.
4. The computer system as recited in claim 22 wherein Q=64, and a 64-bit special register stores bits indicating whether registers in the register files are private registers or global registers, each bit in the 64-bit special register corresponding to one of the registers or global registers, each bit in the 64-bit special register corresponding to one of the registers in the register files.
5. The computer system as recited in claim 23 wherein a plurality of said register files connected to a bus, and a value written to a global register in one of said register files is propagated to a corresponding global register in the other register files connected to the bus across bus.
6. The computer system as recited in claim 24 wherein a plurality of said register files are connected together in serial, and a value written to a first global register in a first of said plurality of register files is propagated to a corresponding global register in a second of said plurality of register files connected directly to said first of said plurality of register files.